Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (09-08)
Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
Application Number	10544894	
Filing Date	2006-07-19	
First Named Inventor	Dasu, Aravind R.	
Art Unit	2193	
Examiner Name	B̶u̶l̶l̶o̶c̶k̶ ̶J̶r̶ ̶L̶e̶w̶i̶s̶ ̶A̶l̶e̶x̶a̶n̶d̶e̶r̶ Tuan Vu	
Attorney Docket Number	117316-155055	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. **Add**

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. **Add**

FOREIGN PATENT DOCUMENTS							Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

		INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		

Application Number	10544894	
Filing Date	2006-07-19	
First Named Inventor	Dasu, Aravind R.	
Art Unit	2193	
Examiner Name	~~Bullock Jr. Lewis Alexander~~	
Attorney Docket Number	117316-155055	

/VAT/	1	Search Report, mailed 03/17/05 for application PCT/US04/03609	☐
/VAT/	2	Abdulrahim, Mohammad A. " Parallel Algorithms for Labeled Graph Matching" PhD thesis Colorado School of Mines, 1998	☐
/VAT/	3	Agarwal, A.et at. "The Raw Compiler Project" Proc of the Second SUIF compiler workshop, Stanford, CA, August 21-23, 1997	☐
/VAT/	4	Agarwal, A., et al. " Routing Architectures for Hierarchical Field Programmable Gate Arrays" IEEE International Conference 071 Computer Design, pp. 475-478, October 10, 1994	☐
/VAT/	5	Akoglu, A., et al. " Pattern Recognition Tool to Detect Reconfigurable Patterns in MPEG4 Video Processing" International Parallel and Distributed Processing Symposium, pp. 131-135, 15-19, April 2002	☐
/VAT/	6	Alsolaim, A., et al. " Architecture and Application of a Dynamically Reconfigurable Hardware Array for Future Mobile Communication Systems" pgs. 205-214	☐
/VAT/	7	Ammons, G., et al. " Exploiting Hardware Performance Counters with Flow and Context Sensitive Profiling" PLDI, June 1997	☐
/VAT/	8	Arnold, M., et al. " Automatic Detection of Recurring Operation Patterns" Seventh International Workshop on Hardware/Software Co-Design (CODES'99), Rome Italy, May 1999	☐
/VAT/	9	Arnold, M., et al. " Instruction Set Synthesis Using Operation Pattern Detection" Fifth Annual Conf. of ASCI, Heijen, The Netherlands, June 1999	☐
/VAT/	10	Arnold, Marnix " Matching and Covering with Multiple-Output Patterns" Technology Report no. 1-68340-44/1999/01, Delft University of Technology, January 1999	☐
/VAT/	11	Athanas, P. "A Functional Reconfigurable Architecture and Compiler for Adaptive Computing" Technical Report LEMS-100, Brown University, Division of Engineering, 1992	☐

		INFORMATION DISCLOSURE STATEMENT BY APPLICANT		

		Application Number	10544894
INFORMATION DISCLOSURE		**Filing Date**	2006-07-19
STATEMENT BY APPLICANT		**First Named Inventor**	Dasu, Aravind R.
(Not for submission under 37 CFR 1.99)		**Art Unit**	2193
		Examiner Name	Bullock Jr Lewis Alexander
		Attorney Docket Number	117316-155055

/VAT/	12	Athanas, P. et al. "An Adaptive Hardware Machine Architecture and Compiler for Dynamic Processor Reconfiguration" International Conference on Computer Design, 1991	☐
/VAT/	13	Ball, T., et al. "Efficient Path Profiling", Proceedings of MICRO-29, December 2-4, 1996, Paris, France	☐
/VAT/	14	Basin, D.A., et al. "A Term Equality Problem Equivalent to Graph Isomorphism" Information Processing Letters, 54: 61-66, 1994	☐
/VAT/	15	Becker, J., et al. "A Parallel Dynamically Reconfigurable Architecture Designed for Flexible Application-Tailored Hardware/Software Systems in Future Mobile Communication" The Journal of Supercomputing, 19 (1), 102-127, 2001	☐
/VAT/	16	Becker, J., et al. "Design and Implementation of a Coarse-Grained Dynamically Reconfigurable Hardware Architecture" IEEE Computer Society Workshop on VLSI, 2001	☐
/VAT/	17	Betz, V., et al. " VPR: A New Packing, Placement and Routing Tool for FPGA Research" International Workshop on Field-Programmable Logic and Application, pp. 213-222, 1997	☐
/VAT/	18	Bittner, R. et al. " Computing Kernels Implemented with a Wormhole RTR CCM" The 5th Annual IEEE Symposium on FPGAs for Custom Computing Machines, 1997	☐
/VAT/	19	Bondalapati, Kiran Kumar " Modeling and Mapping Dynamically Reconfigurable Hybrid Architectures" PhD Thesis, USC, 2001	☐
/VAT/	20	Bozorgzadeh, E., et al. "Rpack: Routability-Driven packing for cluster-based FPGAs" Proceedings of the Conference on Asia South Pacific Design Automation Conference, p. 629-634, January 2001, Japan	☐
/VAT/	21	BRASS Research Group, Berkeley Reconfigurable Architectures, Systems, & Software, http://brass.cs.berkeley.edu	☐
/VAT/	22	Brisk, P. et al." Instruction Generation and Regularity Extraction For Reconfigurable Processors", International Compilers, Architecture and Synthesis for Embedded Systems (CASES), Pages 1-8, October 2002	☐

INFORMATION DISCLOSURE	Application Number	10544894
STATEMENT BY APPLICANT	Filing Date	2006-07-19
	First Named Inventor	Dasu, Aravind R.
(Not for submission under 37 CFR 1.99)	Art Unit	2193
	Examiner Name	Bullock Jr Lewis Alexander
	Attorney Docket Number	117316-155055

/VAT/	23	Brisk, P., et al. " Area-Efficient Instruction Set Synthesis for Reconfigurable System-on-Chip Designs" ACM DAC 2004, pages 395-400 (2004)	☐
/VAT/	24	Brown, Fon R. III " Real-Time Scheduling with Fuzzy Systems, PhD thesis, Utah State University, 1998	☐
/VAT/	25	Cadambi, S., et al. " CPR: A Configuration Profiling Tool" IEEE Symposium on Field-Programmable Custom Computing Machines, (FCCM '99), April 1999, Napa, C	☐
/VAT/	26	Callahan, T. et al. "The Garp Architecture and C Compiler" IEEE Transactions on computers, 2000	☐
/VAT/	27	Cambouropoulos, Emilios "Extracting Significant Patterns from Musical Strings: Some Interesting Problems." London String Days 2000 Workshop, King's College London	☐
/VAT/	28	Campi, F., et al. " A Reconfigurable Processor Architecture and Software Development Environment for Embedded Systems" International Parallel and Distributed Processing Symposium, 2003	☐
/VAT/	29	Chameleon Systems Inc.- www.chameleonsystems.com, "Advanced Communications Technologies- Development Partnership with Chameleon Systems", Business Wire, December 26, 2000	☐
/VAT/	30	Chekuri, C., et al. " Profile-Driven Instruction Level Parallel Scheduling with Application to Super Blocks" Proc of the 29th Annual International Symposium on Microarchitecture (MICRO-29) December, 1996	☐
/VAT/	31	Chen, C., et al. " Unifying Graph Matching Problems with a Practical Solution" In Proceedings of International Conference on Systems, Signals, Control, Computers, September 1998, 55	☐
/VAT/	32	Chen, D., et al. "A Reconfigurable Multiprocessor IC for Rapid Prototyping of Algorithmic-Specific High-Speed DSP Data Paths" IEEE Journal of Solid-State Circuits, 1992	☐
/VAT/	33	Chou, P., et al. "Interval Scheduling: Fine-Grained Code Scheduling for Embedded Systems" Proc. ACM/IEEE DAC, 1995, 462-467	☐

		INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		

Application Number	10544894
Filing Date	2006-07-19
First Named Inventor	Dasu, Aravind R.
Art Unit	2193
Examiner Name	Bullock Jr. Lewis Alexander
Attorney Docket Number	117316-155055

/VAT/	34	Chowdhary, A. "A General Approach for Regularity Extraction in Datapath Circuits", Proc. Of International Conference on Computer-Aided Design, 1998	☐
/VAT/	35	Chu, M.et al. "Object Oriented Circuit-Generators in Java", IEEE Symposium on FPGAs for Custom Computing Machines, April 1998.	☐
/VAT/	36	Coffman, E. , et al. " Optimal Scheduling for Two-Processor Systems" Acta Informatica, 1, 1972, 200-213	☐
/VAT/	37	Cook, D., et al. " Knowledge Discovery from Structural Data" Journal of Intelligent Information Systems, 1995	☐
/VAT/	38	Dasu, A., et al. " An Analysis Tool Set for Reconfigurable Media Processing" The International Conference on Engineering of Reconfigurable Systems and Algorithms, Las Vegas, June 2003	☐
/VAT/	39	Dasu, A., et al. "A Survey of Media Processing Approaches, IEEE Transactions on Circuits and Systems for Video Technology, Vol. 12, NO. 8, August 2002	☐
/VAT/	40	Dasu, Aravind " Reconfigurable Processing" PhD qualifying report 2001	☐
/VAT/	41	De, V., et al. " A Heuristic Global Router for Polycell Layout" PhD thesis, Duke University, 1986	☐
/VAT/	42	Dees, W., et al. " Automated Rip-UP and Reroute Techniques" Proceedings of Design Automation Conference, 1982	☐
/VAT/	43	Dehnert, J., et al. " Compiling for the Cydra-5," Journal of Supercomputing, 7: 181-228 (1993)	☐
/VAT/	44	DeHon, Andre. "Reconfigurable Architectures for General-Purpose Computing", PhD Thesis, MIT, 1996	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	10544894	
	Filing Date	2006-07-19	
	First Named Inventor	Dasu, Aravind R.	
	Art Unit	2193	
	Examiner Name	Bullock, Jr. Lewis Alexander	
	Attorney Docket Number	117316-155055	

/VAT/	45	Dehon, Andre. "The Density Advantage of Configurable Computing" Computer, vol. 33, no. 4, April 2000, pp. 41-49	☐
/VAT/	46	Ebeling, C., et al. "RaPiD- Reconfigurable Pipelines Datapath" Department of Computer Science and Engineering University of Washington	☐
/VAT/	47	Eles, P., et al. " Scheduling of Conditional Process Graphs for the Synthesis of Embedded Systems" Design Automation and Test in Europe, February 23-26, 1998 Paris, France	☐
/VAT/	48	Eles, P., et al. "Scheduling with Bus Access Optimization for Distributed Embedded Systems" IEEE Trans on VLSI Systems, Vol. 8, No. 5, 472-491, October, 2000	☐
/VAT/	49	Fisher, Joseph A. " Global Code Generation For Instruction-Level Parallelism: Trace Scheduling-2" Tech. Rep. HPL 93-43, Hewlett Packard Labs, June, 1993	☐
	50		☐

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/ Tuan A Vu /	Date Considered	7-23-2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.